AMENDMENTS TO THE CLAIMS

~~Claims~~ I claim

Claim 1 (Currently Amended). A method of data processing comprising a method of expanding a data word, the ~~Data~~ data word expansion method for comprising expanding a first, N-digit data word in two's complement representation to produce a second, (N+M)-digit data word, where N and M are natural numbers greater than 0 comprising the steps of

putting the digits in the Nth to 1st place (4, 3) of the first data word into the (N+M)th to (M+1)th place of the second data word such that the digits of the first data word occupy the most significant bit positions of the N + M digits of the second word, retaining the order of digits, and at least one of the first M places of the second data word is set to the logic value "1"[.] , the method further comprising the step of putting the logic value "0" into the Mth place of the second data word.

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Claim 2 (Currently Amended). ~~Method~~ The method according to Claim 1, further comprising the step of setting precisely one of the first M places of the second data word to the logic value "1".

Cancel Claim 3

Claim 4 (Currently Amended). ~~Method~~ The method according to Claim ~~3~~ 1, further comprising putting the logic value "1" into the least significant place of the second data

word, and the logic value "0" into each of the subsequent places up to and including the Mth place.

Claim 5 (Currently Amended). Data processing apparatus ~~Apparatus for~~ configured to extending ~~extend~~ a data word length from N to (N+M) digits, comprising

a first circuit device for outputting an N-digit data word in two's complement representation, the N-digit output of which is connected to the more significant places of an (N+M)-bit-wide data channel, retaining the order of ~~places~~ digits, and

a second circuit device designed for outputting a prescribed M-digit data word having at least one logic value "1", the M-digit output of which is connected to the less significant M places of the (N+M)-bit-wide data channel[.], the Mth place of the M-digit data word having logic value "0".

Claim 6 (Original). The apparatus of Claim 5 further comprising a third circuit device, whose (N+M)-wide input is connected to the (N+M)-wide data channel.